Amendment
Serial No. 10/570236
Attn. Docket no. NL031032

REMARKS

Entry of this Amendment and reconsideration are respectfully requested in view of the amendments made to the claims and for the remarks made herein.

Claims 1-7, 9-13 and 15 are pending in the application and stand rejected.

Claim 1 has been amended.

The Notice Non-Compliant Amendment states that the amendment submitted on October 17, 2008 appears to have a white line through the body of the claims and arguments preventing them from having sufficient clarity and contrast.

In reply Applicant thanks the Examiner for his observation and is at a loss for the reason the submitted document includes a white line.

However, in the interest of advancing the prosecution of the matter, applicant submits, herein, the amendments made to the claims and the arguments provided in the response to the prior Office Action submitted on October 17, 2008.

With regard to the prior Office Action, this Office Action rejected claims 1-7, 9-13 and 15 under 35 USC §103(a) as being unpatentable over Sindhu (USP no. 5,440,698) in view of Foster (USP no. 6,202,007) and further in view of Denneau (USPPA 2003/00287247).

With regard to the rejection of claims 1-7, 9-13 and 15 under 35 USC §103(a) as being unpatentable over Sindhu in view of Foster (USP no. 6,202,007) and further in view of Denneau, applicant respectfully disagrees with and explicitly traverses the reason for rejecting the claims. However, in order to advance the prosecution of this matter, independent claim 1 has been amended to further recite the subject matter claimed in better form and to explicitly recite that at least one local memory unit is selectively accessed according to an address range and that the at least one local memory units corresponding to selected processors. No new matter has been added. Support for the amendment may be found at least on page 9, lines 29-33 ("All data processing units IP are able to access the off-chip memory SDRAM and a further on-chip local memory

January 2009

5

MEM attached to the memory interface MMI, but not all data processing units IP are able to access all on-chip local memories MEM attached to the hubs H_{11}, H_{12} and $H_{2,n}$.

Sindhu (USP no. 5,440,698) discloses an arbitration system for resolving contention on synchronous packet switched busses to ensure that all devices serviced by such a bus are given bounded time access to the bus and to permit such devices to fill all available bus cycles with packets. Flow control for shared memory is implemented by supporting different types of arbitration requests and prioritization of such requests by type. Sindu fails to provide any teaching regarding a single memory space or using memory addresses to distinguish between local and global memory.

Foster (USP no. 6, 202,097) discloses a method for performing diagnostic functions in a multiprocessor data processing system. Foster is cited by the Office Action for teaching a communication interface positioned on a single chip, wherein the memory device is not positioned on the single chip.

Denneau (USPPA no. 2003/0028747) discloses a flexible method for associating cache memories with processors and a main memory wherein an effective address comprises an interest group and an associated address. The interest group represents an index into a cache vector table and/or an entry into the cache vector table. The associated address is used to select one of the caches. In one aspect, only the interest group may be used to represent an address used for access.

The Office Action refers to col. 5, lines 20-23 of Sindhu for teaching a cache-like hierarchy, and col. 16, lines 44-52 for teaching shared write updating "which implies a shared address space." The Office Action further refers to col. 22, line 41- col. 23, line 27 for teaching that when data is not found in lower memory, a higher memory is checked and then the lower level is updated. The Office Action concludes that Sindhu implicitly teaches a shared memory similar to that recited in the claims.

However, a review of the referred to section reveals that Sindu discloses a system wherein the memory is organized with different bit settings to determine the position of data in the cache memories and global memory. See, for example, col. 23, lines 1-54, which state, "[w]henever the second-level cache 19a receives a RBRqst from a resquestor on its cluster bus 15a, the second-level cache 19a may or may not contain a copy of the data block specified by the RBRqst. If it has a copy, the second-level cache returns the

January 2009

6

Amendment
Serial No. 10/570236
Attn. Docket no. NL031032

data to the requestor ... after setting the reply Shared bit in the reply packet to the logically ORed SharedIn value of (a) the SharedOut signals that it receives from the first level caches as a result of the RBRqst and (b) the current state of its shared bit for the specified data block ... If, on the other hand, the second-level cache 19a does not have a copy of the data block that is specified by the RBRqst ... the second-level cache 19a issues a RBRqst packet on the global bus... When a second level cache, such as cache 19a, receives a WSRqst from a requestor on its cluster bus, the cache 19a checks to determine if its shared bit for the data block containing the address specified by the WSRqst is set. If its shared bit for that particular data block is not set, the second level cache 19a updates the data in accordance with the WSRqst, sets its owner bit for the updated block and then issues a WSRply ... via its cluster bus. ..."

Hence, Sinhdu teaches that a check for a copy of the data is made in the memory and if a copy is not available in the local memory (cache) then a next level of memory is checked. However, Sinhdu fails to disclose that the global and local memories are organized such that an address range defines the particular memory. Rather Sindhu performs checks on the data content to determine whether the data is in a lower level and dependent upon the shared bit setting performs additional processing in a higher level memory. Sindu is completely silent with regard to the addressing of each of the memories. And it cannot be implied or considered inherent that the memory is designated over a single memory space.

Foster fails to provide any teaching regarding the use of address ranges for distinguishing global and local memories as is recited in the claims.

Denneau teaches that a range of addresses may be used to define particular cache memory wherein a first range defines a first cache memory that is accessed by a first processor and a second, disjoint, range defines a second cache memory that is accessed by a second processor. Denneau further defines a third, disjoint, range that may be accessed by both the first and second processor (see Figure 3). Thus, Denneau teaches a system wherein a single main memory is divided into a plurality of ranges that may be accessed by processors based on the settings of one or more access bits.

However, the combination of the cited references fails to teach a memory device and at least one local memory units sharing a single address space where local memory

January 2009

7

Amendment
Serial No. 10/570236
Attn. Docket no. NL031032

units are associated with, and accessed by, corresponding processors, as is recited in the claims.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met, 1. there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings, 2. there must be a reasonable expectation of success; and 3. the prior art reference must teach or suggest all the claim limitations.

In this case, a *prima facie* case of obviousness has not been made as each of the elements recited in the claims is not disclosed by the combination of Sindhu, Foster and Denneau.

For the amendments made to the independent claims and for the remarks made herein, applicant submits that the rejection of the independent claim 1 has been overcome and respectfully requests that the rejection be withdrawn.

With regard to the remaining claims, these claims depend from independent claim 1, which has been shown to include subject matter not disclosed by the combination of Sindhu, Foster and Denneau. Consequently, the remaining dependent claims are also not rendered obvious by Sindhu, Foster and Denneau as the remaining dependent claims also include subject matter not disclosed by the cited references.

For the amendments made to the claims and for the remarks made herein, applicant submits that all the objections and rejections have been overcome and that the claims are in a condition for allowance. Applicant respectfully requests that a Notice of Allowance be issued.
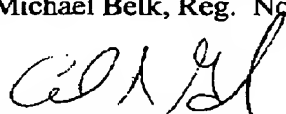
January 2009

8

Amendment
Serial No. 10/570236
Attn. Docket no. NL031032

No fee is believed necessary for filing this response to the Notice of Non-Compliant Amendment. However, if any fees are deemed necessary, the Examiner is authorized to charge Deposit Account no. 50-4414.

Should the Examiner believe that the disposition of any issues arising from this response may be best resolved by a telephone call, the Examiner is invited to contact applicant's representative at the telephone number listed below.

Respectfully submitted,
Michael Belk, Reg. No. 33,357

Date: January 21, 2009
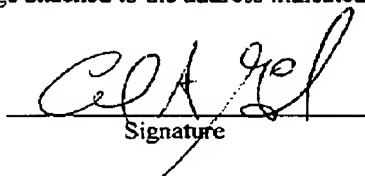
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January 2009